Application No. 10/688,122

Amendments to the Claims:

Please cancel Claim 1 and add new Claims 2-23. This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (New) A circuit for reducing mismatches between the outputs from successive pairs of cells in an analog to digital converter, comprising:

a plurality of cells each having a first input terminal, a second input terminal, a first output terminal and a second output terminal;

a voltage input means, coupled to a first input terminal of each cell, introducing an input voltage to the first input terminal;

a reference voltage means, coupled to the second input terminal of each cell, for producing progressive fractions of a reference voltage at each of the second input terminals;

a low impedance means, coupled between corresponding first output terminals in successive cells, and coupled between corresponding second output terminals in successive cells, drawing load-bearing currents to the successive cells to affect the relative voltages on the first output terminal and the second output terminal and reduce the effects of cell mismatches on the output terminals; and

a high impedance means, coupled to the each of the first output terminals in successive cells and to each of the second

output terminals in successive cells, for providing a high impedance relative to an impedance provided by said low impedance means.

3. (New) The circuit of Claim 2, wherein the circuit is formed as an integrated circuit on a chip.

4. (New) The circuit of Claim 2, wherein the reference voltage means is comprised of a reference voltage source means connected to a continuous strip of impedance material.

5. (New) The circuit of Claim 2, wherein the low impedance means is comprised of a continuous strip of impedance material.

6. (New) The circuit of Claim 2, wherein the outputs from successive cells are read in sequence in accordance with the progressive fractions of the reference voltage introduced to such cells.

7. (New) The circuit of Claim 2, wherein the high impedance means coupled to the cells has an impedance approaching infinity to draw the load bearing currents though the low impedance means.

8. (New) The circuit of Claim 2, wherein the cells in the plurality are divided into subsets, the output terminals in corresponding cells in the different subsets having common connections to the low impedance.

9. (New) The circuit of Claim 8, wherein the cells in alternate subsets are folded relative to the cells in the other subsets.

10. (New) The circuit of Claim 8, wherein the cells in alternate subsets have outputs changing at increases in the progressive fractions of the reference voltage means in a particular direction relative to the direction of the changes in the outputs of the cells in the other subsets.

11. (New) The circuit of Claim 9, wherein the outputs of the cells are cascaded by providing an additional folding of such outputs.

12. (New) The circuit of Claim 10, wherein the outputs of the cells are cascaded by changing such outputs in a particular direction for a first group of successive outputs and then in a second direction opposite to the first direction for a second group of successive outputs immediately following the outputs in the first group.

13. (New) A circuit for reducing mismatches between the outputs from successive pairs of differential amplifiers in an analog to digital converter, comprising:

a plurality of differential amplifiers each having a first input terminal, a second input terminal, a first output terminal and a second output terminal;

a voltage input, coupled to a first input terminal in each of the differential amplifiers, for introducing an input voltage to the first input terminals;

a reference voltage, coupled to the second one of the input terminals in each of the differential amplifiers, for producing progressive fractions of a reference voltage to each of the second input terminals;

a low impedance, coupled between corresponding first output terminals in successive differential amplifiers, and coupled

between corresponding second output terminals in successive differential amplifiers, drawing load-bearing currents to the successive differential amplifiers to affect the relative values of the first output terminal and the second output terminal and reduce the effects of amplifier mismatches on the output terminals; and

a high impedance, coupled to the each of the first output terminals in successive differential amplifiers and to each of the second output terminals in successive differential amplifiers, providing a high impedance relative to an impedance provided by said low impedance.

14. (New) The circuit of Claim 2, wherein the circuit is formed as an integrated circuit on a chip.

15. (New) The circuit of Claim 13, wherein the reference voltage means is comprised of a reference voltage source means connected to a continuous strip of impedance material.

16. (New) The circuit of Claim 13, wherein the low impedance means is comprised of a continuous strip of impedance material.

17. (New) The circuit of Claim 13, wherein the outputs from successive differential amplifiers are read in sequence in accordance with the progressive fractions of the reference voltage introduced to such differential amplifiers.

18. (New) The circuit of Claim 13, wherein the high impedance means coupled to the differential amplifiers has an impedance approaching infinity to draw the flow of the load bearing currents though the low impedance means.

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19. (New) The circuit of Claim 13, wherein the differential amplifiers in the plurality are divided into subsets, the output terminals in corresponding differential amplifiers in the different subsets having common connections to the low impedance.

20. (New) The circuit of Claim 19, wherein the differential amplifiers in alternate subsets are folded relative to the differential amplifiers in the other subsets.

21. (New) The circuit of Claim 19, wherein the differential amplifiers in alternate subsets have outputs changing at increases in the progressive fractions of the reference voltage means in a particular direction relative to the direction of the changes in the outputs of the differential amplifiers in the other subsets.

22. (New) The circuit of Claim 20, wherein the outputs of the differential amplifiers are cascaded by providing an additional folding of such outputs.

23. (New) The circuit of Claim 21, wherein the outputs of the differential amplifiers are cascaded by changing such outputs in a particular direction for a first group of successive outputs and then in a second direction opposite to the first direction for a second group of successive outputs immediately following the outputs in the first group.